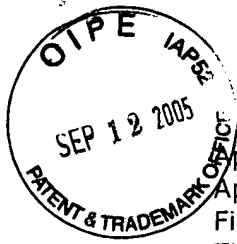


IFW



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Appln. No: 10/772,611  
Applicant: Hiroyuki Senda et al.  
Filed: 02/05/2004  
Title: ERROR CORRECTION CIRCUIT AND ERROR CORRECTION METHOD  
TC/A.U.: 2133  
Examiner: Joseph D. Torres  
Confirmation No.: 5071  
Docket No.: YAO-4210US1

**RESPONSE**

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

S I R :

This is in response to the Office Letter dated **June 8, 2005**, please reexamine the above-identified application in view of the remarks set forth below.

**REMARKS**

Claims 41 and 42 are pending.

**Objection to the Specification**

The disclosure is objected to on informal grounds. According to the Office Action, claims 41 and 42 recite "the received trellis-encoded signal having  $2^S$  internal states", and also recite "a signal having  $2^{(S+1)}$  internal states", but the specification does not teach us such features. Applicants respectfully disagree.

It is Applicants' position that the specification provides a very detailed description of the error correction method and the error correction circuit defined respectively in independent claims 41 and 42. In this connection, Applicants submit that support for the above-noted features are found throughout the specification. But in particular direct the Examiner's attention to the disclosure between pages 37 and 62 as well as the Figures associated with this detailed description (See Figures 1-21).

In particular Applicants point out that in a Final Office Action directed to the parent application, U.S. Patent Application No. 09/311,394 filed May 13, 1999,